ABSTRACT OF THE DISCLOSURE

Self-aligned split-gate flash memory cell array and process of fabrication in which erase and select gates are positioned on opposite sides of stacked floating and control gates, with source regions in the substrate beneath the erase gates, bit line diffusions which are partially overlapped by select gates at the ends of the rows of the cells. The floating and control gates are self-aligned with each other, and the erase and select gates are split from but self-aligned with the stacked gates. With the floating gates surrounded by the other gates and the source regions, high voltage coupling for both programming and erase operations is significantly enhanced. The memory cells are substantially smaller than prior art cells, and the array is biased so that all of the memory cells in it can be erased simultaneously, while programming is bit selectable.